

Claims

What is claimed is:

1. A method for transferring data between a host device and a storage medium, comprising:
 - receiving from the host device a command to transfer data between the host device and the storage medium;
 - storing in a first register a value for tracking a number of data units that have been transferred into a buffer but that have not yet been transferred out of the buffer;
 - modifying a value contained in the first register in response to a transfer of a data unit into the buffer; and
 - modifying a value contained in the first register in response to a transfer of a data unit out of the buffer.
2. The method of claim 1, further comprising:
 - storing in a second register a value for incrementing a value contained in the first register; and
 - incrementing a value contained in the first register by the value contained in the second register.
3. The method of claim 1, further comprising:
 - storing in a third register a value for decrementing a value contained in the first register; and
 - decrementing a value contained in the first register by the value contained in the third register.
4. The method of claim 1, further comprising:
 - storing in a fourth register an address representing a location in the buffer where data is being transferred between the buffer and the host device; and
 - storing in a fifth register an address representing a location in the buffer where data is being transferred between the buffer and the storage medium.

1 5. The method of claim 4, further comprising:

2 storing in a sixth register an address representing a beginning of the
3 buffer; and
4 storing in a seventh register an address representing an end of the
5 buffer.

1 6. The method of claim 5, further comprising:

2 storing in an eighth register a value representing a storage capacity of
3 the buffer.

1 7. The method of claim 1, wherein the host device is a computer.

1 8. The method of claim 1, wherein the storage medium comprises non-volatile
2 semiconductor memory.

1 9. The method of claim 1, further comprising:

2 implementing the method via an application specific integrated circuit
3 (ASIC).

1 10. A data transfer system for transferring data between a host device and a
2 storage medium, comprising:

3 a host interface that receives from the host device a command to
4 transfer data between the host device and the storage medium;
5 a buffer that temporarily stores data that is transferred between the host
6 device and the storage medium;
7 a first register that stores a value for tracking a number of data units
8 that have been transferred into the buffer but that have not yet
9 been transferred out of the buffer;
10 a second register that stores a value for incrementing a value contained
11 in the first register; and
12 a third register that stores a value for decrementing a value contained
13 in the first register.

- 1 11. The data transfer system of claim 10, wherein the data transfer system is
2 configured to modify a value contained in the first register in response to a
3 transfer of a data unit between the buffer and the host device.

- 1 12. The data transfer system of claim 11, wherein the data transfer system is
2 configured to modify a value contained in the first register in response to a
3 transfer of a data unit between the buffer and the storage medium.

- 1 13. The data transfer system of claim 10, wherein the data transfer system is
2 configured to increment a value contained in the first register by the value
3 contained in the second register.

- 1 14. The data transfer system of claim 13, wherein the data transfer system is
2 configured to decrement a value contained in the first register by the value
3 contained in the third register.

- 1 15. The data transfer system of claim 10, further comprising:
2 a fourth register that stores an address representing a location in the
3 buffer where data is being transferred between the buffer and
4 the host device; and
5 a fifth register that stores an address representing a location in the
6 buffer where data is being transferred between the buffer and
7 the storage medium.

- 1 16. The data transfer system of claim 15, further comprising:
2 a sixth register that stores an address representing a beginning of the
3 buffer; and
4 a seventh register that stores an address representing an end of the
5 buffer.

- 1 17. The data transfer system of claim 16, further comprising:
2 an eighth register that stores a value representing a storage capacity of
3 the buffer.

- 1 18. The data transfer system of claim 10, wherein the data transfer system is an
2 application specific integrated circuit (ASIC).
- 1 19. A method for transferring data between a host device and a storage medium,
2 comprising:
3 receiving from the host device a command to transfer data between the
4 host device and the storage medium;
5 storing in a first register a value for determining a buffer's fullness;
6 incrementing a value contained in the first register by a value
7 contained in a second register; and
8 decrementing a value contained in the first register by a value
9 contained in a third register.
- 1 20. The method of claim 19, further comprising:
2 incrementing a value contained in the first register by the value
3 contained in the second register in response to a data transfer
4 into the buffer.
- 1 21. The method of claim 19, further comprising:
2 decrementing a value contained in the first register by the value
3 contained in the third register in response to a data transfer out
4 of the buffer.
- 1 22. An application specific integrated circuit (ASIC) for transferring data between
2 a host device and a storage medium, comprising:
3 a buffer that temporarily stores data that is transferred between the host
4 device and the storage medium;
5 a first register that stores a value for determining the buffer's fullness;
6 a second register that stores a value for incrementing a value contained
7 in the first register; and
8 a third register that stores a value for decrementing a value contained
9 in the first register.

1 23. The ASIC of claim 22, wherein the data transfer system is configured to
2 increment a value contained in the first register by the value contained in the second
3 register in response to a data transfer into the buffer.

1 24. The ASIC of claim 22, wherein the data transfer system is configured to
2 decrement a value contained in the first register by the value contained in the
3 third register in response to a data transfer out of the buffer.

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